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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,459	DAVIS ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7 and 9-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 9-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/24/2008, 7/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5, 7, and 9-37 are pending in this office action and presented for examination. Claims 1, 5, 7, 9, 14-16, 20-21, 24-26, 29, 31, 32, and 35 are newly amended and claims 6 and 8 are newly cancelled by amendment filed 7/11/2008

Double Patenting

2. Claims 1-5, 7, 9-14, 16, 18, 22-23, 25, 31-35 of this application conflict with claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of Application No. 10715370. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-5, 7, 9-14, 16, 18, 22-23, 25, and 31-35 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of copending Application No. 10715370. Although the conflicting claims are not identical, they are not patentably distinct from each other because each particular instant claim is an obvious variant of the corresponding claim of the '370 application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. All limitations of claim 1 of the instant application are taught in claim 1 of the '370 application except the one or more peripherals; however, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine a peripheral with the instant claim in order to, for example, interact with the CPU.

a. All further limitations of claim 2 of the instant application are also taught in claim 1 of the '370 application.

b. All further limitations of claim 3 of the instant application are also taught in claim 1 of the '370 application.

c. All further limitations of claim 4 of the instant application are also taught in claim 8 (dependent on claim 1) of the '370 application.

d. All further limitations of claim 5 of the instant application are taught in claim 2 (dependent on claim 1) of the '370 application.

e. All further limitations of claim 7 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application except that the PCE comprises programming code; however, it would have been obvious to one of ordinary skill in the art at the time of the invention that an engine can be implemented as either software or hardware.

f. All further limitations of claim 9 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application.

g. All further limitations of claim 10 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application except that the PPM is high-speed and is connected to one of the DME and the FPE by a high-speed data bus; however, it would have been obvious to one of ordinary skill in the art at the time of the invention that a high-speed memory would lead to greater system performance, that a data bus would be able to be used to connect two components, and that the data bus being high-speed would also lead to greater system performance.

h. All further limitations of claim 11 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application, as some form of memory interface is inherent given a memory connected to a data bus.

i. All further limitations of claim 12-13 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application, as a PPU operatively

connected to a CPU entails some form of connection, and it would have been obvious to one of ordinary skill in the art at the time of the invention for this connection to be a bus, as well as for a bridge to be used to connect an internal and external bus.

j. All further limitations of claim 14 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application.

k. All further limitations of claim 16 of the instant application are taught in claim 7 (dependent on claim 1) of the '370 application.

l. All further limitations of claim 18 of the instant application are taught in claim 7 (dependent on claim 1) of the '370 application.

6. All limitations of claim 22 and 23 of the instant application are taught in claim 20 (which is dependent on claims 17 and 18) of the '370 application except for limitations which are obvious variants of claim 20 of the '370 application which are explained above.

7. All limitations of claim 25 of the instant application are taught in claim 15 of the '370 application except for limitations which are obvious variants of claim 15 of the '370 application which are explained above.

8. All limitations of claim 31 of the instant application are taught in claim 23 of the '370 application except for limitations which are obvious variants of claim 23 of the '370 application which are explained above.

9. All further limitations of claims 32 and 33 of the instant application are taught in claim 27 of the '370 application.

10. All further limitations of claims 34 of the instant application are taught in claim 23 of the '370 application.

11. All further limitations of claims 35 of the instant application are taught in claim 30 of the '370 application.

12. Claims 1-5, 7, 9-14, 16, 18, 20, 22-23, 25, and 29-36 of this application conflict with claims 2, 8, and 19 of Application No. 10715440. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

13. Claims 1-5, 7, 9-14, 16, 18, 20, 22-23, 25, and 29-36 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2, 8, and 19 of copending Application No. 10715440. Although the conflicting claims are not identical, they are not patentably distinct from each other because each particular instant claim is an obvious variant of the corresponding claim of the '440 application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

14. The rationale for these rejections are similar to the rejection using the '370 application above. To summarize:

m. The limitations of claims 1-4 of the instant application are obvious variants of claim 2 of the '440 application.

n. The limitations of claims 9-14, 16, 18, 22-23, 25, and 29-37 of the instant application are obvious variants of claim 19 of the '440 application.

o. The limitations of claim 20 of the instant application are obvious variants of claim 8 of the '440 application.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. Claims 1-5, 7, and 9-37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

17. Claims 1, 25, and 31 recite the limitation "a Data Movement Engine configured to…initiate context switches relative to one or more other system elements" in the last 4 lines. However, the instant specification appears to disclose that the context switches are only applicable to the DME and FPE. As the scope of the instant limitation is

greater than the associated disclosure in the specification, it does not appear that the applicant at the time the application was filed had possession of initiating context switches relative to one or more of any other system elements, rather than just solely the DME and FPE.

p. Claims 2-5, 7, 9-24, 26-30, and 32-37 are rejected for failing to alleviate the rejection of claims 1, 25, and 31 above.

18. Claim 14 recites the limitation "an Inter-engine Memory (IEM)...configured to...initiate a context switch in response to commands received from the DME" in lines 2-4. However, the original disclosure does not appear to disclose of the IEM being able to initiate a context switch in response to commands received from the DME.

q. Claims 15-18 and 20-21 are rejected for failing to alleviate the rejection of claim 14 above.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-4, 7, 9-15, 18-19, 22-23, 25-27, 29-31, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook et al. (Van Hook) (US 6342892 B1)

in view of Bishop et al. (Bishop) (Sparta: Simulation of Physics on a Real-Time Architecture).

21. Consider claim 1, Van Hook discloses a Central Processing Unit (CPU) (Figure 2, main processor 100) operatively connected to an external memory (Figure 2, video game storage device 54) and one or more peripherals (Figure 2, game controllers); and, a coprocessor (Figure 2, coprocessor 200), wherein the coprocessor includes: a PPU Control Engine (PCE) (Figure 5, CPU interface 202) configured to control the execution of commands (col. 7, lines 4-9, optimized for rapid processing) and to communicate with a software driver executing on the CPU (Figure 2, the CPU interface provides communication to the main processor; see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers. Alternatively, the PCE can be the signal processor 400 of Figure 5), a Physics Processing Memory (PPM) coupled to the CPU (Figure 5, memory 300), a Data Movement Engine (DME) configured to transfer data between the coprocessor and at least one coprocessor internal memory in response to commands received from the PCE (col. 17, lines 17-19, DMA circuit; also, see col. 22, lines 13-15, signal processor retrieves additional SP microcode modules from main memory as needed to perform the specified tasks…may use its DMA facility) and to initiate context switches relative to one or more other system elements (this limitation can be met in multiple ways. Col. 19, lines 40-57 disclose that both execution unit 430 and main processor 100 can command the DMA facility. Col. 20, lines 6-8, disclose that DMA status registers are read by main processor to determine whether DMA controller 454 is full or busy. Therefore, for

example, the DMA status registers determine whether a DMA controller can or cannot switch and process the DMA request of the main processor context relative to the signal processor, and vice versa. Alternatively, col. 17, line 30-42 disclose that the DMA controllers of each sub-block can all independently access main memory using shared busses. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that, for example, the DMA controller of the signal processor will not attempt to take control of the bus if it has no data to access, and the DMA controller of the signal processor will attempt to take control of the bus at some point if it does have data to access. Therefore, the DMA controller of the signal processor is determining whether one of the shared buses switches the system element it is servicing from one of the other elements of col. 17, lines 17-29 to the signal processor).

However, Van Hook does not explicitly disclose that the coprocessor is a Physics Processing Unit (PPU) configured to provide force and collision computations on real-time physics simulation data.

On the other hand, Bishop does disclose of a Physics Processing Unit configured to provide force and collision computations on real-time physics simulation data (Figure 1, ideal SPARTA implementation; section 1 discloses of physical modeling of solid objects through the use of specialized hardware; section 2 and section 3.1 discloses of collision detection and force computation).

Bishop's teaching of using specialized hardware accelerates physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments (Bishop, section 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that this combination would entail either the implementation of a co-processor architecture of Van Hook for the purpose of physical modeling as cited above, or the modification of the existing co-processor architecture of Van Hook to support physical modeling capabilities.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments.

22. Consider claim 2, Van Hook discloses the CPU comprises a processing unit resident in a personal computer (col. 6, line 51, computer).

23. Consider claim 3, Van Hook discloses the CPU comprises a processing unit resident in a game console (col. 1, lines 13-14, video game systems).

24. Consider claim 4, Van Hook discloses of a Graphics Processing Unit (GPU) operatively connected to the CPU (Figure 2, display processor 500).

25. Consider claim 7, Van Hook discloses the PCE (Figure 5, signal processor 400 comprises programming code stored in a memory resident within the PPU (Figure 5, microcode RAM 402).

26. Consider claim 9, Van Hook as modified by Bishop discloses a Floating Point Engine (FPE) configured to respond to commands from at least one of the PCE and the DME, and to execute floating point computations (Bishop discloses in page 5 of floating point units; Van Hook in col. 18, lines 8-11, discloses of execution units responsive to instructions residing instruction memory).

27. Consider claim 10, Van Hook discloses that the PPM comprises a high-speed memory and the PPU further comprises a high-speed data bus connecting the high-speed memory to at least one of the DME and the FPE (Figure 5, RDRAM 200, bus 106 explained in col. 15, lines 1-3, Figure 5 also shows data being stored).

28. Consider claim 11, Van Hook discloses a memory interface unit managing data communication between the high- speed data bus and the high-speed memory (Figure 5, DRAM controller/Interface).

29. Consider claim 12, Van Hook discloses a processor bus connecting the PCE with at least one physical interface to the CPU (Figure 5, bus 214).

30. Consider claim 13, Van Hook discloses the processor bus is separate from the high-speed bus and connected to the high-speed bus via a bridge (Figure 5, wherein the dram controller/interface 212 acts as the bridge).

31. Consider claim 14, Van Hook as modified by Bishop discloses an Inter-Engine Memory (IEM) coupled to the DME and the FPE and configured to receive physics simulation data from the PPM and to initiate a context switch in response to commands received from the DME (Figure 6, instruction memory 402 or data memory 404, see col. 19, lines 41-50, wherein the instruction memory containing an instruction which requires data from the main memory using DMA essentially initiates the context switch as described in the independent claim, wherein that instruction is itself loaded from main memory based on load instructions sent to the DMA).

32. Consider claim 15, Van Hook discloses an Inter-Engine Register (IER) coupled to the DME and the FPE and adapted to initiate DME operation in responsive to a PCE command (see, for example, col. 19, lines 60-67, SP-DRAM DMA address register 458 can be written to from SP execution unit and is used to specify a starting DMA address within instruction memory or data memory; alternatively, the program counter can also read on the inter-engine register).

33. Consider claim 18, Van Hook discloses a Scratch Pad Memory (SPM) receiving data from the PPM in response to commands from the DME (Figure 6, instruction memory 402 or data memory 404, see col. 19, lines 41-50).

34. Consider claim 19, Van Hook discloses a DME control interface comprising: a first packet queue receiving command packets from the PCE and communicating command packets to the DME; and, a second packet queue receiving response packets from the DME and communicating the response packets to the PCE (col. 19, lines 61-67 and col. 20, lines 1-8, data can be both written to and read from the memory; the SP-DRAM DMA address register serves as the first packet queue and the data memory in the signal processor is the second packet queue, or the buffer of col. 61, line 19).

35. Consider claim 22, Van Hook discloses the FPE further comprises: a plurality of floating point operation execution units (Bishop discloses in page 5 of floating point units; Van Hook in col. 18, lines 8-11, discloses of execution units responsive to instructions residing instruction memory).

36. Consider claim 23, Van Hook as modified by Bishop discloses the plurality of floating point execution units are selectively grouped together to form a vector floating point unit (Bishop discloses in page 5 of floating point units; Van Hook in col. 18, lines 8-11, discloses of execution units responsive to instructions residing instruction memory and of vector operation in col. 16, lines 7-9).

37. Consider claim 25, Van Hook discloses a host (Figure 1, system 50), wherein the host comprises an external memory (Figure 2, video game storage device 54) and a peripheral (Figure 2, game controllers) operatively connected to a Central Processing Unit (CPU) (Figure 2, main processor 100) and, a coprocessor operatively connected to the CPU (Figure 2, coprocessor 200), wherein the coprocessor includes: a PPU Control Engine (PCE) (Figure 5, CPU interface 202) configured to control the execution of commands (col. 7, lines 4-9, optimized for rapid processing) and to communicate with a software driver executing on the CPU (Figure 2, the CPU interface provides communication to the main processor; see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers. Alternatively, the PCE can be the signal processor 400 of Figure 5), a Physics Processing Memory (PPM) coupled to the CPU (Figure 5, memory 300), a Data Movement Engine (DME) configured to transfer data between the coprocessor and at least one coprocessor internal memory in response to commands received from the PCE (col. 17, lines 17-19, DMA circuit; also, see col. 22, lines 13-15, signal processor retrieves additional SP microcode modules from main memory as needed to perform the specified tasks...may use its DMA facility) and to initiate context switches relative to one or more other system elements (this limitation can be met in multiple ways. Col. 19, lines 40-57 disclose that both execution unit 430 and main processor 100 can command the DMA facility. Col. 20, lines 6-8, disclose that DMA status registers are read by main processor to determine whether DMA controller 454 is full or busy. Therefore, for example, the DMA

status registers determine whether a DMA controller can or cannot switch and process the DMA request of the main processor context relative to the signal processor, and vice versa. Alternatively, col. 17, line 30-42 disclose that the DMA controllers of each sub-block can all independently access main memory using shared busses. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that, for example, the DMA controller of the signal processor will not attempt to take control of the bus if it has no data to access, and the DMA controller of the signal processor will attempt to take control of the bus at some point if it does have data to access. Therefore, the DMA controller of the signal processor is determining whether one of the shared buses switches the system element it is servicing from one of the other elements of col. 17, lines 17-29 to the signal processor); wherein the host stores a main game program (col. 4, lines 35-37, video game storage device 54) and a PPU driver; and, wherein the PPU driver manages all communication between the PPU and the CPU (see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

However, Van Hook does not explicitly disclose that the coprocessor is a Physics Processing Unit (PPU) configured to provide force and collision computations on real-time physics simulation data.

On the other hand, Bishop does disclose of a Physics Processing Unit configured to provide force and collision computations on real-time physics simulation data (Figure 1, ideal SPARTA implementation; section 1 discloses of physical modeling of solid

objects through the use of specialized hardware; section 2 and section 3.1 discloses of collision detection and force computation).

Bishop's teaching of using specialized hardware accelerates physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments (Bishop, section 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that this combination would entail either the implementation of a co-processor architecture of Van Hook for the purpose of physical modeling as cited above, or the modification of the existing co-processor architecture of Van Hook to support physical modeling capabilities.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments.

38. Consider claim 26, Van Hook discloses a first Application Programming Interface (API) associated with the main game program (col. 13, lines 13-16, software architecture/constructs to implement video game program 108 in a high level software environment); and a second API associated with the PPU driver (see, for example, col.

8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

39. Consider claim 27, Van Hook discloses the second API is callable by the first API (col. 13, lines 13-16, software architecture/constructs to implement video game program 108 in a high level software environment; see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

40. Consider claim 29, Van Hook as modified by Bishop discloses of a dedicated vector processor adapted to perform parallel floating point operations (Bishop discloses in page 5 of floating point units; Van Hook in col. 18, lines 8-11, discloses of execution units responsive to instructions residing instruction memory and of vector operation in col. 16, lines 7-9).

41. Consider claim 30, Van Hook discloses the PPU further comprises a high-speed memory (Figure 5, RDRAM 200).

42. Consider claim 31, Van Hook discloses a personal computer system (PC) (Figure 1, system 50) executing a game program (Figure 2, video game storage device 54, the instructions of which are executed) on hardware comprising a memory (Figure 2, video game storage device 54), a peripheral (Figure 2, game controllers), and a general purpose microprocessor (Figure 2, main processor 100); and, a coprocessor (Figure 2,

coprocessor 200), wherein the coprocessor includes: a PPU Control Engine (PCE) (Figure 5, CPU interface 202) configured to control the execution of commands (col. 7, lines 4-9, optimized for rapid processing) and to communicate with a software driver executing on the general purpose microprocessor (Figure 2, the CPU interface provides communication to the main processor; see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers. Alternatively, the PCE can be the signal processor 400 of Figure 5), a Physics Processing Memory (PPM) coupled to the CPU (Figure 5, memory 300), a Data Movement Engine (DME) configured to transfer data between the coprocessor and at least one coprocessor internal memory in response to commands received from the PCE (col. 17, lines 17-19, DMA circuit; also, see col. 22, lines 13-15, signal processor retrieves additional SP microcode modules from main memory as needed to perform the specified tasks...may use its DMA facility) and to initiate context switches relative to one or more other system elements (this limitation can be met in multiple ways. Col. 19, lines 40-57 disclose that both execution unit 430 and main processor 100 can command the DMA facility. Col. 20, lines 6-8, disclose that DMA status registers are read by main processor to determine whether DMA controller 454 is full or busy. Therefore, for example, the DMA status registers determine whether a DMA controller can or cannot switch and process the DMA request of the main processor context relative to the signal processor, and vice versa. Alternatively, col. 17, line 30-42 disclose that the DMA controllers of each sub-block can all independently access main memory using shared busses. It would have been readily recognized to one of ordinary skill in the art at the time of the

invention that, for example, the DMA controller of the signal processor will not attempt to take control of the bus if it has no data to access, and the DMA controller of the signal processor will attempt to take control of the bus at some point if it does have data to access. Therefore, the DMA controller of the signal processor is determining whether one of the shared buses switches the system element it is servicing from one of the other elements of col. 17, lines 17-29 to the signal processor)..

However, Van Hook does not explicitly disclose that the coprocessor is a dedicated Physics Processing Unit (PPU) adapted to compute physics simulation data for incorporation within execution of the game program.

On the other hand, Bishop does disclose of a Physics Processing Unit adapted to compute physics simulation data (Figure 1, ideal SPARTA implementation; section 1 discloses of physical modeling of solid objects through the use of specialized hardware).

Bishop's teaching of using specialized hardware accelerates physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments (Bishop, section 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that this combination would entail either the implementation of a co-processor architecture of Van Hook for the purpose of physical modeling as cited above, or the modification of the existing co-processor

architecture of Van Hook to support physical modeling capabilities. It would have been readily recognized t one of ordinary skill in the art at the time of the invention that the teaching of Bishop, as applied to Van Hook, would be able to be incorporated within execution of the game program.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments.

43. Consider claim 34, Van Hook discloses the general purpose microprocessor generates a command in response to execution of the game program and communicates the command to the PPU (see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

44. Claims 5, 32-33, and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook and Bishop as applied to claim 1, 31, and 34 above, and further in view of Intel (Intel PCI and PCI Express; note that the subject matter relied upon in the reference is dated).

45. Consider claim 5, Van Hook does not disclose that the CPU and PPU communicate via at least one selected from a group of physical interfaces consisting of: Universal Serial Bus (USB), USB2, Firewire, Peripheral Component Interconnect (PCI), Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI-Express interface (pages 2-3, PCI, PCI Express).

The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the PCI-Express interface supports important features such as power management and the ability to handl both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and it is noted in Figure 2 of Van Hook as modified by Bishop that there exists a bus that connects the CPU and the PPU.

46. Consider claim 32, Van Hook does not disclose that the PPU is operatively connected within the PC by means of an expansion board.

On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI-Express interface (pages 2-3, PCI, PCI Express). Moreover, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that a device that connects to a PCI interface is an expansion board.

The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the

PCI-Express interface supports important features such as power management and the ability to handle both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and it is noted in Figure 2 of Van Hook as modified by Bishop that there exists a bus that connects the CPU and the PPU.

47. Consider claim 33, Van Hook discloses a Graphics Processing Unit (GPU) adapted to compute graphics data for incorporation within execution of the game program (Van Hook, Figure 5, SP 400 or display processor 500).

48. Consider claim 35, Van Hook does not disclose that the PPU and general purpose microprocessor communicate via at least one selected from a group of physical interfaces consisting of: Universal Serial Bus (USB), USB2, Firewire, Peripheral Component Interconnect (PCI), Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI-Express interface (pages 2-3, PCI, PCI Express).

The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the

PCI-Express interface supports important features such as power management and the ability to handl both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and it is noted in Figure 2 of Van Hook as modified by Bishop that there exists a bus that connects the CPU and the PPU.

49. Consider claim 36, Van Hook discloses the PPU comprises a vector processor adapted to run parallel floating point operations (Bishop discloses in page 5 of floating point units; Van Hook in col. 18, lines 8-11, discloses of execution units responsive to instructions residing instruction memory and of vector operation in col. 16, lines 7-9).

50. Claim 16-17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook and Bishop as applied to claim 14 above, and further in view of Dakhil (US 6341318 B1)

51. Consider claim 16, Van Hook and Bishop do not disclose that the IEM comprises multiple banks of memory adapted to support parallel threads of execution.

On the other hand, Dakhil does disclose of using a multiple bank memory to support parallel threads of execution (the steps of col. 2, lines 15-44).

Dakhil's teaching increases the efficiency of data processing system by minimizing idle processing iterations.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dakhil with the invention of Van Hook and Bishop in order to increase data processing efficiency by minimizing idle processing iterations. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the environment of Dakhil is similar to the environment of Van Hook and Bishop, as both Dakhil and the combination of Van Hook and Bishop involve DMA transactions and memory accessible from more than one source.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dakhil with the invention of Van Hook and Bishop in order to increase data processing efficiency by minimizing idle processing iterations.

52. Consider claim 17, Van Hook discloses the IER comprises multiple registers

However, Van Hook and Bishop do not disclose that the IEM and IER are a multiple bank memory and register respectively adapted to support two parallel threads of execution.

On the other hand, Dakhil does disclose of using a multiple bank memory to support two parallel threads of execution (the steps of col. 2, lines 15-44).

Dakhil's teaching increases the efficiency of data processing system by minimizing idle processing iterations.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dakhil with the invention of Van Hook and Bishop in order to increase data processing efficiency by minimizing idle processing iterations. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the environment of Dakhil is similar to the environment of Van Hook and Bishop, as both Dakhil and the combination of Van Hook and Bishop involve DMA transactions and memory accessible from more than one source.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dakhil with the invention of Van Hook and Bishop in order to increase data processing efficiency by minimizing idle processing iterations.

53. Consider claim 20, Van Hook as modified by Dakhil discloses a Scratch Pad Memory (SPM) receiving data from the PPM in response to commands from the DME (Figure 6, instruction memory 402 or data memory 404, see col. 19, lines 41-50), wherein the IEM further comprises a first bank accessible to the DME and a second bank accessible to the FPE (col. 2, lines 15-39 as above); and, wherein the DME further comprises: a first unidirectional crossbar connected to the first bank (col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the external device and the first memory area, the outputs are the banks of the IEM; this crossbar encompasses the read address signals), a second unidirectional crossbar connected to the second bank (col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the banks of the IEM, the

outputs are the external device and the first memory area; this crossbar encompasses the write address signals); and, a bi-directional crossbar connecting first and second crossbars to at least one of the PPM or SPM (col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the data from each bank of the IEM, the outputs are the external device and the first memory area; also see Figure 7 of Van Hook, Register files. Also see col. 15, lines 22-24, communication between components).

54. Consider claim 21, Van Hook discloses a first Address Generation Unit providing Read address data to the first unidirectional crossbar (col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the external device and the first memory area, the outputs are the banks of the IEM; this crossbar encompasses the read address signals); and, a second Address Generation Unit providing Write address data to the second unidirectional crossbar (col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the banks of the IEM, the outputs are the external device and the first memory area; this crossbar encompasses the write address signals).

55. Claims 24 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook and Bishop as applied to claim 23 and 34 above, and further in view of Shiell et al. (Shiell) (6317820).

56. Consider claim 24, Van Hook and Bishop do not disclose the FPE performs floating point operations in response to a Very Long Instruction Word (VLIW).

On the other hand, Shiell does disclose of VLIW instructions (col. 1, lines 50-62, VLIW word, a number of different instruction streams are statically scheduled together).

VLIWs are highly effective for regular, loop-oriented tasks such as are typical of the performance-sensitive aspects of digital signal processing and other "number-crunching" applications (Shiell, col. 1, lines 40-43). Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that VLIW CPUs offer significantly more computational power, thus increasing system performance.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Shiell with the invention of Van Hook and Bishop in order to increase system performance. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the physical modeling of Bishop is one example of a "number-crunching" application (see Bishop, section 3.1, title overview, computationally intensive)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Shiell with the invention of Van Hook and Bishop in order to increase system performance.

57. Consider claim 37, Van Hook and Bishop do not disclose the command is a Very Long Instruction Word (VLIW).

On the other hand, Shiell does disclose of VLIW instructions (col. 1, lines 50-62, VLIW word, a number of different instruction streams are statically scheduled together).

VLIWs are highly effective for regular, loop-oriented tasks such as are typical of the performance-sensitive aspects of digital signal processing and other "number-crunching" applications (Shiell, col. 1, lines 40-43). Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that VLIW CPUs offer significantly more computational power, thus increasing system performance.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Shiell with the invention of Van Hook and Bishop in order to increase system performance. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the physical modeling of Bishop is one example of a "number-crunching" application (see Bishop, section 3.1, title overview, computationally intensive)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Shiell with the invention of Van Hook and Bishop in order to increase system performance.

58. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook as applied to claim 27 above, and further in view of Telekinesys (Havok Game Dynamics SDK; note that although this particular reference is dated 2002, the base Havok platform predates this reference).

59. Consider claim 28, Van Hook discloses a Graphics Processor Unit (GPU), wherein the host further stores: a GPU driver and a third API associated with the GPU driver (Van Hook, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers) wherein the second API would be callable by the first API (see claim 27 above).

Although Bishop discloses that the Sparta can be integrated with graphics hardware (section 3.4, bullet point 3), based on which examiner believes it would have been obvious that the second API is callable by the third API, Bishop nevertheless does not explicitly disclose this as he does not elaborate on the term "integrated".

On the other hand, Telekinesys explicitly discloses that the second API is callable by the third API (see, for example, page 19, section 11, interface to the physics system, industry standard graphics API). Also see the first paragraph of section 11, "the first thing any game developer needs to do when using a physics engine is to interface the physics system to the existing 3d graphics / rendering solution."

Bishop teaches that integrating the physics co-processor with the graphics hardware avoids a bottleneck between the CPU and graphics hardware (Bishop, section 3.4, bulletpoint 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Telekinesys with the invention of Van Hook and Bishop in order to avoid a bottleneck between the CPU and graphics hardware. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results,

and it is readily seen that the interfacing of Telekinesys would be able to be modularly substituted with the broad integration as taught by Bishop.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Telekinesys with the invention of Van Hook and Bishop in order to avoid a bottleneck between the CPU and graphics hardware.

Response to Arguments

60. Applicant argues that Van Hook discloses in col. 19, lines 41-57 that the DMA module is commanded not by the signal processor but by either the main processor or an execution unit. However, the execution unit 430 is part of the signal processor; see, for example, Figure 7. Therefore, in Van Hook, the signal processor can command the DMA module.

Applicant also argues that the DMA module as disclosed in Van Hook does not initiate context switches relative to one or more elements of the system. However, as explained in the rejection above, a broad interpretation of the aforementioned limitation enables Van Hook to teach the limitation in two different ways.

Conclusion

61. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 6:15 a.m. - 5:45 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

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Examiner, Art Unit 2183